PATENT
AMENDMENT UNDER FINAL REJECTION
EXPEDITED PROCEDURE EXAMINING GROUP 2100

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 09/697,305	)	Confirmation No. 4222
In re Application of	)	Group Art Unit: 2133
Takaki YOSHIDA et al.	)	Examiner: Joseph D. Torres
Filed: October 27, 2000	)	

For: FAULT DETECTING METHOD AND LAYOUT METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT

AMENDMENT UNDER 37 CFR 1.116

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Sir:

In response to the Office Action mailed October 24, 2005, please undertake the following changes:

1/30/2006